

TWINNING PROGRESS

GOVERNMENT COLLEGE OF ENGINEERING,SALEM, TAMILNADU (MENTOR INSTITUTION)

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GOVERNMENT ENGINEERING COLLEGE ,RAIPUR, CHHATTISGARH (MENTEE INSTITUTION)



TWINNING ACTIVITIES

S.NO	TITLE OF THE PROGRAMME	DATE
1	Dr.M.Raja, AP/Mechanical, Government College of Engineering ,Salem attended Two day workshop on "Start-up activities & preparation of action plan" at CET, Bhubaneswar along with Mentee institute.	29.12.2017 & 30.12.2017
2	Dr.A.K.Dubey,Principal,Government Engineering College, Raipur, Dr.Y.P. Banjare, TEQIP Coordinator GEC Raipur, Mr.KHP Ram, ,TEQIP Administrator, GEC Raipur visited Government College of Engineering , Salem for twinning activities under TEQIP-III	05.02.2018 & 06.02.2018
3	Dr.K.Logavani, AP/EEE & Dr.T.R.Sumithra ,AP/EEE ,Government College of Engineering, Salem attended two day workshop on "Outcome Based Education (OBE) for Engineering Programs" along with Mentee institute at AICTE auditorium, NewDelhi-Organized by NPIU.	08.02.2018 & 09.02.2018

S.NO	TITLE OF THE PROGRAMME	DATE
4	Dr.G.Vimala Rosaline, Principal, GCE Salem, Dr.R.Shanmugalakshmi, Professor/EEE, GCE Salem, Dr.R.Vijayan, Professor/Mechanical, GCE Salem Visited Government Engineering College, Raipur for twinning activities under TEQIP-III.	15.02.2018 & 16.02.2018
5	Faculty members from Mentee Institution visited Mentor Institution for discussions about – E-SAR Preparation, NBA files preparation and submission and study about facilities available in various departments.	26.04.2018 & 27.04.2018
6	Five Faculty Members from Government Engineering College, Raipur attended one week Faculty Development programme under TEQIP-III on "Embedded Systems and VLSI Design" at Government College of Engineering, Salem	to

Mentor Institution Members visit to GEC, Raipur on 15.02.2018 & 16.02.2018

Mentee Institution Faculty members visit to GCE, Salem on 26.04.2018 & 27.04.2018



Faculty Development programme under TEQIP-III on "Embedded Systems and VLSI Design"



Faculty Development programme under TEQIP-III on "Embedded Systems and VLSI Design"

